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IEEE JNL IEEE Journal or Magazine

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Iwata, Y.; Hyashi, S.; Satoh, R.; Fujimoto, K.;  
[Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-E Micro-Systems, 2005. EuroSimE 2005. Proceedings of the 6th International Cc](#)  
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Digital Object Identifier 10.1109/ESIME.2005.1502833  
[AbstractPlus](#) | Full Text: [PDF](#)(457 KB) IEEE CNF  
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Adya, S.N.; Markov, I.L.;  
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)  
Volume 11, Issue 6, Dec. 2003 Page(s):1120 - 1135  
Digital Object Identifier 10.1109/TVLSI.2003.817546  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1310 KB) IEEE JNL  
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- ☐ 3. **Modern Floorplanning Based on \$rm B^ast\$-Tree and Fast Simulated Ann**  
Chen, T.-C.; Chang, Y.-W.;  
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction](#)  
Volume 25, Issue 4, April 2006 Page(s):637 - 650  
Digital Object Identifier 10.1109/TCAD.2006.870076  
[AbstractPlus](#) | Full Text: [PDF](#)(856 KB) IEEE JNL  
[Rights and Permissions](#)
- ☐ 4. **Fixed-outline floorplanning through better local search**  
Adya, S.N.; Markov, I.L.;  
[Computer Design, 2001. ICCD 2001. Proceedings. 2001 International Confere](#)  
23-26 Sept. 2001 Page(s):328 - 334  
Digital Object Identifier 10.1109/ICCD.2001.955047  
[AbstractPlus](#) | Full Text: [PDF](#)(632 KB) IEEE CNF  
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- ☐ 5. **An efficient algorithm to fixed-outline floorplanning based on Instance au**  
Rong Liu; Sheqin Dong; Xianlong Hong;  
[Computer Aided Design and Computer Graphics, 2005. Ninth International Co](#)  
7-10 Dec. 2005 Page(s):6 pp.